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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Garg *et al.*

Appl. No. 09/188,708

Filed: November 10, 1998

For: **RISC Microprocessor Architecture Implementing Multiple Typed Register Sets**

Art Unit: 2783

Examiner: L. Donaghue

Atty. Docket: SP018.C4

Attention: <u>Box Non-Fee Amendment</u>

Second Preliminary Amendment

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

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Prior to examination of the above-captioned application and calculation of a filing fee, please enter the following Amendment.

In the Claims:

Please amend claim 31 as follows:

--31.   (Amended)   A processor, comprising:

an execution unit that performs at least one operation according to an instruction;

a first register set including a plurality of first registers each for holding integer data; and

a second register set including a plurality of second registers each for holding said integer data and for holding floating point data,

wherein said instruction [specific] <u>specifies</u> which of said first and second register sets is to be accessed, and wherein said execution unit accesses said first register set or said second register set as specified by said instruction, reads an operand value from either said first register